

[illegible][illegible]

DOW ISSUE	CO ISSUE	DATE	BLIND	APPRO
1	1	2-6-79	2000	1000
2A	2A	2-7-79	2000	1000

SUPPORTING INFORMATION		SHEET INDEX NOTES
CATEGORY	NO.	
EQUIPMENT DWG	009559AS	1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
EQUIPMENT DESIGN REQS	009550 (001-008-155)	2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THIS DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
		3. THE ISSUE NUMBER ASSIGNED TO A CHANGE OF NEW SHEET WILL BE THE SHEET ISSUE NUMBER AS THAT OF THE SHEET INDEX.
		4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
		5. THE LAST ISSUE NUMBER OF THE SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

NOTICE- NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

CCWOM SYSTEMS SWITCHED MAINTENANCE ACCESS SYSTEM NO. 5B INTERFACE CIRCUIT		IN19 AT&TCO STANDARD
DWG SIZE 65		ISSUE 2A 9 SHEETS
BELL LABORATORIES	SD-9964-01-	

APPARATUS INDEX

DESIG	LOCATION	
	FS	APP FIG. EXP'T
RELAYS		
6M	2A3	1
CTT	1E9	1
DF1	1E6	1
DF2	1E6	1
LT		
SEL	2E3	1
SPAR	2E3	1
SPAT	2E3	1
SPAR		
SPAT	2F3	1
SPC	2F1	1

CAPACITORS

MA	296	1
MB	296	1

DIODES

6M	2A3	1
CT	2E2	1
CTT	1E9	1
DF1	1E6	1
DF2		
LT	2E3	1
LTS	2F3	1
SEL	2E3	1
SP	2F2	1
SPC	2F1	1

TRANSFORMERS

MA	296	1
MB	296	1

LEAD INDEX

DESIG.	LOCATION	
	FS	CAD
CONTROLLER & CONNECTION CXT		
AC)	209	1C0,102
BC)	209	1C0,102
CC)	209	1C0,102
CC)	2C1	102
DE)		
DE)	209	1C0,102
EE)	209	1C0,102
FE)	209	1C0,102
GE)	209	1C0,102
HE)		
HE)	209	1C0,102
IE)	209	102
JE)	209	102
KE)	209	102
LE)		
LE)	209	102
ME)	209	102
NE)	2C1	1C0,102
RE)	1F9	1C0,102
SE 1A0-1		
SE 1A0-1	2C1	2E0
SE 1A1-1	2C1	2E0
SE 1A1-2	2C1	2E0
SE 1B0-1		
SE 1B0-1	2C1	2E0
SE 1B1-1	2C1	2E0
SE 1B1-2	2C1	2E0
SE 1C0-1		
SE 1C0-1	2C1	2E0
SE 1C1-1	2C1	2E0
SE 1C1-2	2C1	2E0

DESIG	LOCATION	
	FS	CAD
RTS 5A REMOTE TEST POST		
CC)		
CH)		
CH)		
EE)		
EN)		
FE)		
GE)		
HE)		
IE)		
JE)		
KE)		
LE)		
ME)		
NE)		
RE)		
SE)		
TE)		
TI)		

DESIG	LOCATION	
	FS	CAD
RTS 5A LOCAL TEST PORTS AND DISTRIBUTION CXT		
CC)	1E0	100
CH)	1A3,1E0	105,100
CH)	1A3,1E0	105,100
EE)	1E0	100
EE)	1A3,1E0	105,100
EE)	1A3,1E0	105,100
EN)	1A3,1E0	105,100
FE)	1E0	100
GE)	1E0	100
HE)	1E0	100
HE)	1A3,1E0	105,100
HE)	1A3,1E0	105,100
ME)	1A3,1E0	105,100
NE)	1E0	100
NE)	1A3,1E0	105,100
RE)	1E0	100
RE)	1A3,1E0	105,100
TE)	1E0	100
TE)	1A3,1E0	105,100
TI)	1A3,1E0	105,100

OPTION INDEX

APP DUE	RATED ON ISSUE	REF NOTES	LOCATION

INTERFACE CIRCUIT

DWG SIZE
A2ISSUE
2A

BELL LABORATORIES

SD-99641-01-

A2

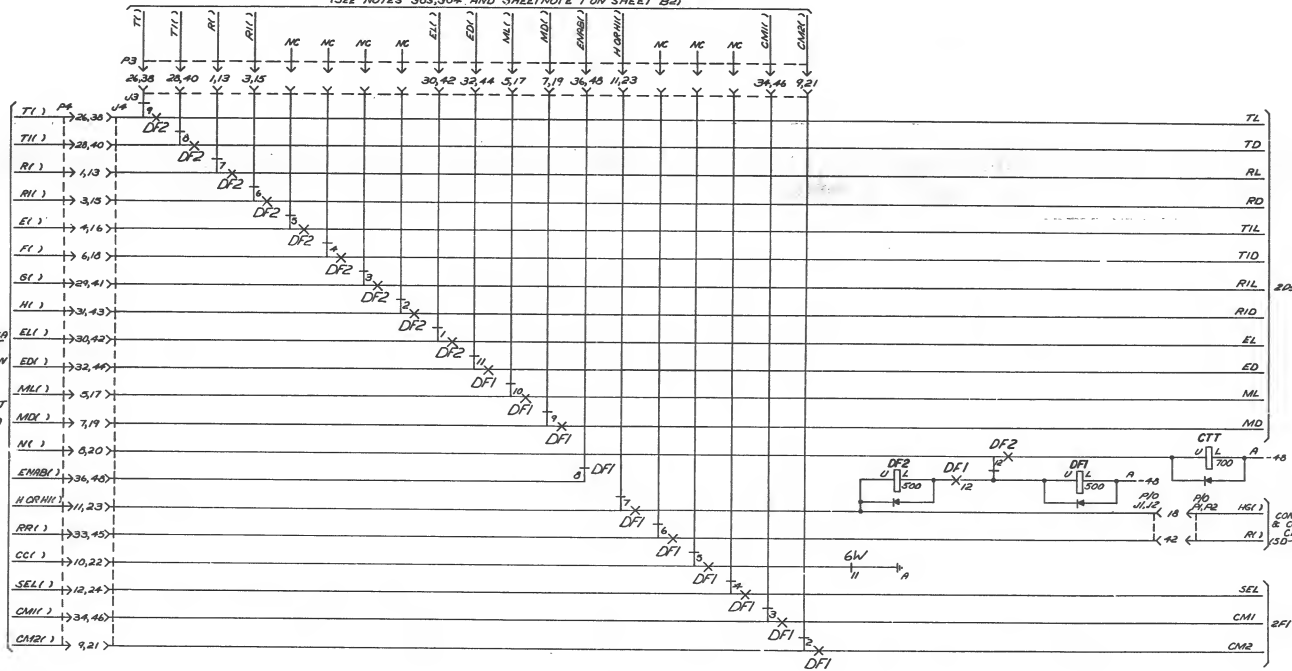
FS I STEERING AND CUT-THROUGH CKT

NOTES:

1. THE () IN THE LEAD DESIGNATION WILL TAKE THE SAME NUMBER AS THE TEST PORT. - IN LEAD (1) CONNECTED TO TEST PORT 4 WILL BE DESIGNATED (4).

TO SMAS NO. 58 LOCAL TEST PORTS AND DISTRIBUTION CATTED (IP04-01)
(SEE NOTES 303, 304, AND 305 SHEET NOTE 1 ON SHEET 05)

TO
SMAS NO. 58
LOCAL TEST
PORTS AND
DISTRIBUTION
CIRCUIT
(SD-IP04-01)
OR
RIS 3A
REMOTE TEST
PORT
(SD-IP08-01)
(SEE NOTE
AND 305)

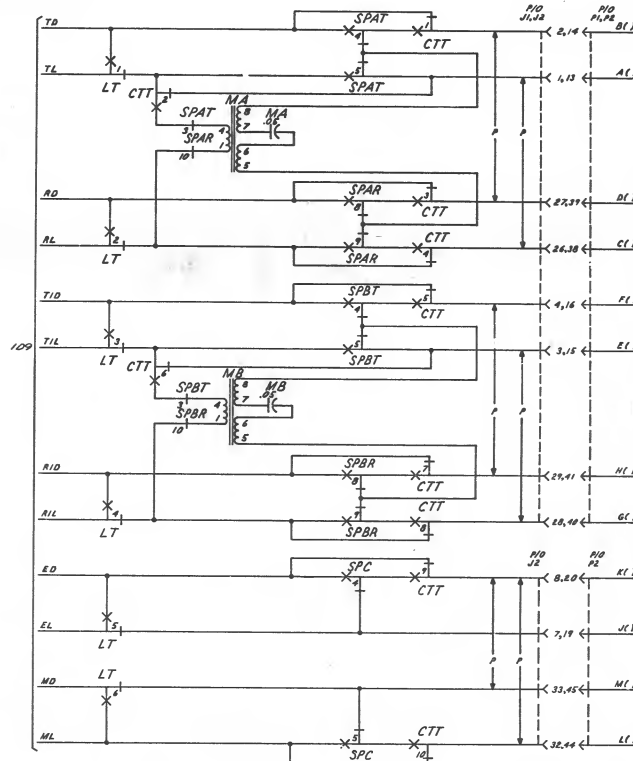
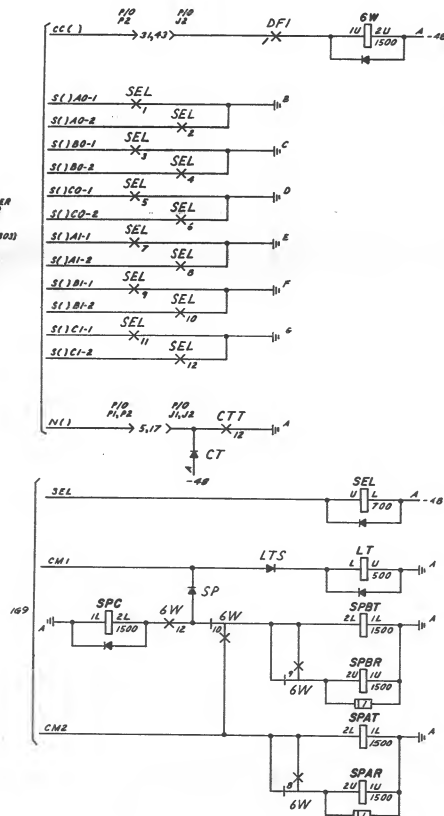


NOTICE- NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

INTERFACE CIRCUIT		DWG SIZE 65	ISSUE 2A
BELL LABORATORIES		SD-99641-01	-BI

FS 2 CONTROL & MONITOR CIRCUIT

TO CONTROLLER & CONNECTOR
CIRCUIT
(SD-9960-01)
(SEE NOTE 7 & 303)



TO CONTROLLER & CONNECTOR
CIRCUIT
(SD-9960-01)
(SEE NOTE 1 & 301)

NOTES:

1. THE () IN THE LEAD DESIGNATION WILL TAKE THE SAME NUMBER AS THE INTERFACE CIRCUIT. NO LEAD BE CONNECTED TO INTERFACE CIRCUIT 4 WILL BE DESIGNATION B(A).

NOTICE- NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

INTERFACE CIRCUIT

DWG SIZE
AS

ISSUE
2A

BELL LABORATORIES SD-99641-01-

82

APP FIG.1

RELAY		MTD/H(SPC)												MTD/H (M)													
DESIG	6M	CTT	DF1	DF2	LT		SEL	SPAR	SPAT	SPHX	SPIT	SPC	DESIG	6M	CTT	DF1	DF2	LT		SEL	SPAR	SPAT	SPHX	SPIT	SPC	DESIG	
CODE	1/2K47	AJ12	AJ81	AJ81	AJ81		AJ12	AK47		AK47		1/2K47	CODE	1/2K47	AJ12	AJ81	AJ81	AJ81		AJ12	AK47		AK47		1/2K47	CODE	
OPTION													OPTION													OPTION	
CON ARR	LOC	CON ARR	LOC	CON ARR	LOC	CON ARR	LOC	CON ARR	LOC	CON ARR	LOC	CON ARR	LOC	CON ARR	LOC	CON ARR	LOC	CON ARR	LOC	CON ARR	LOC	CON ARR	LOC	CON ARR	LOC	CON ARR	LOC
12	N	2F2	EM	202	EM	1E7	EM	1E7	EM	EM	202	N														12	
11	EM	1F6	EM		EM	1E3	EM		EM	EM	201	EM														11	
10	EM	2F2	EM	207	EM	1E4	EM		EM	EM	2C2	EM	206	EM												10	
9	EM	203	EM	2E7	EM	1E4	EM	1C1	EM		EM	2C1	EM	2C7	EM											9	
8	EM	203	EM	2E7	EM	1E4	EM	1C1	EM		EM	2C2	EM	2B7	EM											8	
7			EM	2-7	EM	1E4	EM	1C2	EM		EM	2C1		EM	2E7											7	
6			EM	205	EM	1F5	EM	1C2	EM		EM	2C2														6	
5			EM	2C7	EM	1F5	EM	1C2	EM		EM	2B7		EM	207	EM	207	EM	207	EM	207	EM	207	EM	207	EM	5
4			EM	2C7	EM	1G5	EM	1G5	EM		EM	2B2		EM	2E7	EM	2C7	EM	2F7	EM	2F7	EM	2F7	EM	2F7	EM	4
3			EM	2C7	EM	1G5	EM	1G5	EM		EM	2B1		EM	206	EM										3	
2			EM	2B5	EM	1G6	EM	1G5	EM		EM	2B2		EM		EM										2	
1			EM	2A7	EM	2A2	EM	1G5	EM		EM	2B1		M		M										1	
COIL	2B3	1E9	1E8	1E8	1E8	2E3	2E3	2E3	2E3	2E3	2E3	2E3	2E3	2F3	2F3	2F3	2F3	2F3	2F3	2F3	2F3	2F3	2F3	2F3	2F3	COIL	

CAPACITOR

DESIG LOC CODE
 MA 206 KS-20400 L2, 0.05
 MB 206 KS-20400 L2, 0.05

RIBBE

DESIG LOC CODE
 MA 2E3 S53A
 CT 2E2 S53F
 CTT 1E9 S53A
 DF1 1E9 S53A
 DF2 1E6 S53A
 LT 2E3 S53A
 L7S 2F2 S53F
 SEL 2E3 S53A
 SP 2F2 S53F
 SPC 2F1 S53A

NETWORK

DESIG	LOC	CODE	DESIG	LOC	CODE
SPAR	203	185A	MA	206	2536AC
SPAR	2F3	161A	MB	206	2536AC

TRANSFORMER

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INTERFACE CIRCUIT

DWG SIZE
 65
 ISSUE
 2A

BELL LABORATORIES

SD-99641-01-

CI

CIRCUIT NOTES:

191.

[illegible]

CIRCUIT NOTES: (CONT)

103

RECORD OF APP. FIGURES, WIRING AND APPARATUS CHANGES						
CHANGED ON ISS	IF JOB RECORDS DO NOT SPECIFY	THIS OPTION WAS FURN	SEE NOTE	USE IN CIRCUIT		
				STD	ADM	WD

EQUIPMENT NOTES:

201. CONNECTORIZED CABLES SHALL BE OF THE A25C TYPE OR EQUIVALENT TO MATE WITH CORRESPONDING CONNECTORS ON J99359A5-1 AND OTHER EQUIPMENTS. LENGTH SHALL BE SPECIFIED BY THE JOB SPECIFICATION.

INFORMATION NOTES:

301. UNLESS OTHERWISE SPECIFIED;
RESISTANCE VALUES ARE IN OHMS,
CAPACITANCE VALUES ARE IN MICROFARADS.
VALUES PRECEDED BY THE SYMBOL + (PLUS) OR
- (MINUS) ARE IN VOLTS.

302. INTERFACE CIRCUITS WILL BE NUMBERED CONSECUTIVELY FROM 0 TO 19.

303. FOR ASSIGNING CONNECTIONS FROM INTERFACE CIRCUITS TO TEST PORTS (50-1P108-01 OR 50-1P108-01) AND THE CONTROLLER AND CONNECTOR CIRCUIT (50-99560-01) THE INTERFACE CIRCUIT 0 IS CONNECTED TO TEST PORT 1 AND LEVEL 0 OF SWITCH CONNECTOR 0-0, INTERFACE CIRCUIT 1 IS CONNECTED TO TEST PORT 2 AND LEVEL 1 OF SWITCH CONNECTOR 0-0, INTERFACE CIRCUIT 2 IS CONNECTED TO TEST PORT 3 AND LEVEL 2 OF SWITCH CONNECTOR 0-0, INTERFACE CIRCUIT 3 IS CONNECTED TO TEST PORT 4 AND LEVEL 3 OF SWITCH CONNECTOR 0-0, INTERFACE CIRCUIT 4 IS CONNECTED TO TEST PORT 5 AND LEVEL 4 OF SWITCH CONNECTOR 0-0, INTERFACE CIRCUIT 5 IS CONNECTED TO TEST PORT 6 AND LEVEL 5 OF SWITCH CONNECTOR 0-0, INTERFACE CIRCUIT 6 IS CONNECTED TO TEST PORT 7 AND LEVEL 6 OF SWITCH CONNECTOR 0-0, INTERFACE CIRCUIT 7 IS CONNECTED TO TEST PORT 8 AND LEVEL 7 OF SWITCH CONNECTOR 0-0, INTERFACE CIRCUIT 8 IS CONNECTED TO TEST PORT 9 AND LEVEL 8 OF SWITCH CONNECTOR 0-0, INTERFACE CIRCUIT 9 IS CONNECTED TO TEST PORT 10 AND LEVEL 9 OF SWITCH CONNECTOR 0-0, INTERFACE CIRCUIT 10 IS CONNECTED TO TEST PORT 11 AND LEVEL 0 OF SWITCH CONNECTOR 0-0A, - - - INTERFACE CIRCUIT 19 IS CONNECTED TO TEST PORT 20 AND LEVEL 9 OF SWITCH CONNECTOR 0-0A.

304. FOR ASSIGNING CONNECTIONS FROM INTERFACE CIRCUITS TO THE
LOCAL TEST PORT AND DISTRIBUTION CIRCUIT (50-1106-01)
INTERFACE CIRCUIT 0 IS CONNECTED TO THE STAGE 00
DISTRIBUTION NETWORK MODULE 0 VERTICAL 0, INTERFACE CIRCUIT
1 IS CONNECTED TO THE STAGE 00 DISTRIBUTION NETWORK MODULE
0 VERTICAL 1, - - - INTERFACE CIRCUIT 9 IS CONNECTED TO
THE STAGE 00 DISTRIBUTION NETWORK MODULE 0 VERTICAL 9,
INTERFACE CIRCUIT 10 IS CONNECTED TO THE STAGE 00 DISTRI-
BUTION NETWORK MODULE 1 VERTICAL 0, - - - INTERFACE CIRCUIT
19 IS CONNECTED TO THE STAGE 00 DISTRIBUTION NETWORK MODULE
1 VERTICAL 9.

102.

1047

NETWORK VALUES		
NETWORK NO.	RESISTANCE IN OHMS	CAPACITANCE IN UF
1	470	0.11

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INTERFACE CIRCUIT

ONG SI

ISSUE

45

2A

BELL LABORATORIES

SD-99641-01-

DI

APPARATUS				CIRCUIT REQUIREMENTS										REMARKS				
DESG	CODE	OPT	FVS	MECH REET			CIRCUIT PREPARATION				SEE TEST NOTE	DIRECT CURRENT FLOW REET						
				SDP FVS	CONF FVS	ASLT TRVL	BLOCK OR ISOLATE	TEST CLIP DATA	TEST CONN BAT.	TEST CLIP GRD		TEST WIDE	TEST FOR		TEST SOUR MA	TEST READJ MA	TEST READJ MA	
RELAY																		
AH	1/2847			202					U(SW)	GRD	1	0	13.2	12.5			MTD WITH (SPC)	
CTT	AJ12			220					U(CTT)	GRD		0	41	40.5				
DF1	AJ81			220					U(DF1)	GRD		0	26.5	25				
DF2	AJ81			220					L(DF8) U(DF2)	B/S		0	24.5	23				
LT	AJ81			210					L(LT)	BAT.		0	26.5	25				
SEL	AJ12			220					U(SEL)	GRD		0	43	40.5				
SP8B	1/2847			202					8(W)	20(SP8B)	BAT.	1	0	13.2	12.5		MTD WITH (SP81)	
SP8E	1/2847			202					8(W)	2L(SP8E)	BAT.	1	0	13.2	12.5		MTD WITH (SP8B)	
SP8B	1/2847			202					9(W)	2L(SP8B)	BAT.	1	0	13.2	12.5		MTD WITH (SP8T)	
SP81	1/2847			202					9(W)	2L(SP81)	BAT.	1	0	13.2	12.5		MTD WITH (SP8B)	
SPC	1/2847			202					2L(SPC)	BAT.	1	0	13.2	12.5			MTD WITH (G4)	

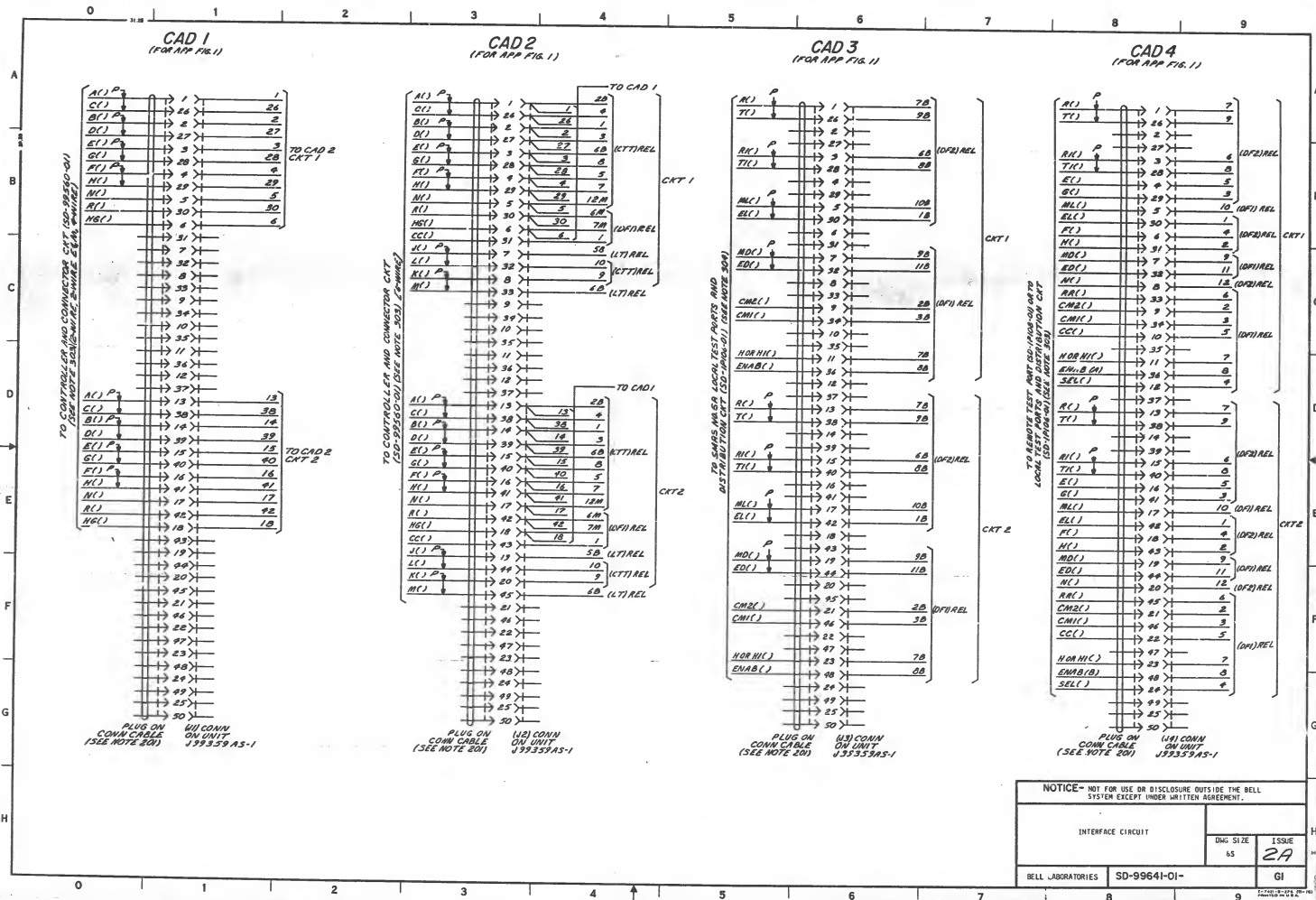
1. ARMATURE BACK TENSION MINIMUM 20 GRAMS READJUST: 15 GRAM TEST.

ISSUE

SD-99641-01-FI

BELL TELEPHONE LABORATORIES
INCORPORATED

69



CAD 5
(FOR APP FIG. 1)

TO CONTROLLER IN CONNECTOR CIRCUIT (SD-99641-01) (SEE NOTE 303)

SI 1A0-1	1M
SI 1B0-1	3M
SI 1A0-1	1M
SI 1B0-1	3M
SI 1C0-1	5M
SI 1C0-1	5M
SI 1A0-2	2M
SI 1B0-2	4M
SI 1A0-2	2M
SI 1B0-2	4M
SI 1C0-2	6M
SI 1C0-2	6M
SI 1A1-1	7M
SI 1B1-1	9M
SI 1A1-1	7M
SI 1B1-1	9M
SI 1C1-1	11M
SI 1C1-1	11M
SI 1A1-2	8M
SI 1B1-2	10M
SI 1A1-2	8M
SI 1B1-2	10M
SI 1C1-2	12M
SI 1C1-2	12M

TO FRAME FUSE PANEL

GRD A-	U (LT) REL
GRD B-	1
GRD C-	3
GRD D-	5
GRD E-	7 (ISEL) REL
GRD F-	9
GRD G-	11
GRD A-	U (LT) REL
GRD B-	1
GRD C-	3
GRD D-	5
GRD E-	7 (ISEL) REL
GRD F-	9
GRD G-	11

TS(1) ON UNIT 10033485-1

TO FRAME FUSE PANEL

193	0
189	0
178	0
168	0
159	0
149	0
139	0
129	0
119	0
109	0
99	0
89	0
79	0
69	0
59	0
49	0
39	0
29	0
19	0
09	0
03	0
192	0
182	0
172	0
162	0
152	0
142	0
132	0
122	0
112	0
102	0
92	0
82	0
72	0
62	0
52	0
42	0
32	0
22	0
12	0
02	0

TO FRAME FUSE PANEL

195	0
185	0
175	0
165	0
155	0
145	0
135	0
125	0
115	0
105	0
95	0
85	0
75	0
65	0
55	0
45	0
35	0
25	0
15	0
05	0
01	0
05	0
15	0
25	0
35	0
45	0
55	0
65	0
75	0
85	0
95	0
105	0
115	0
125	0
135	0
145	0
155	0
165	0
175	0
185	0
195	0

NOTICE- NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

INTERFACE CIRCUIT	
DWG SIZE 6S	ISSUE 2A
BELL LABORATORIES	SD-99641-01
G2	

INTERFACE CIRCUIT

DWG SIZE	ISSUE
6S	2A

BELL LABORATORIES	SD-99641-01-
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G2

《中国书画函授大学肇庆分校建校二十周年纪念册》
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